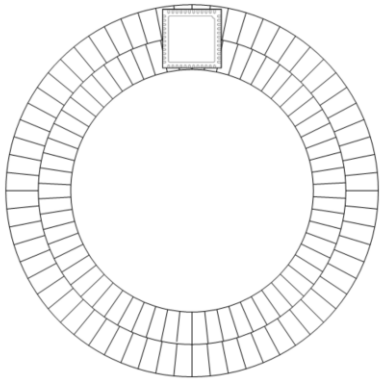
NSM3502 High-Precision Off-Axis Magnetic Encoder Evaluation Board

Product Specification



Magnetic Ring Mounting Diagram

1. Overview & Key Features

The NSM3502 Evaluation Board (EVB) developed by OTV Sensing is a professional evaluation kit based on the NSM3502 — NOVOSENSE's next-generation integrated high-precision off-axis angle and position sensor chip built on Hall array technology. The board integrates power management, signal decoupling and filtering, push-button reset and status indicator circuits, and brings out all core signal interfaces, enabling engineers to rapidly evaluate and develop for motor control, robot joints and industrial automation applications.

1.1 Core Working Principle

The NSM3502 integrates a dual-track vernier Hall sensing array (main-track pole pitch of 2 mm). When a magnetic scale or an off-axis magnet ring with a main-track pole pitch of 2 mm rotates or moves above the chip's Hall array, the two internal Hall arrays sense the magnetic field changes and output sine and cosine analog voltage signals that vary with position. The analog signals are amplified by a high-gain analog front-end (PGA) and low-pass filtered, then quantized by an analog-to-digital converter (ADC). A high-precision digital signal processor (DSP) compensates the quantized sine/cosine values for amplitude, offset and phase, solves the electrical angle, and computes a 22-bit high-precision absolute angle over the full 360° range using the vernier algorithm.

1.2 Core Features

- Off-axis detection: dual-track vernier Hall array architecture, suitable for off-axis and hollow-shaft mechanical installations.

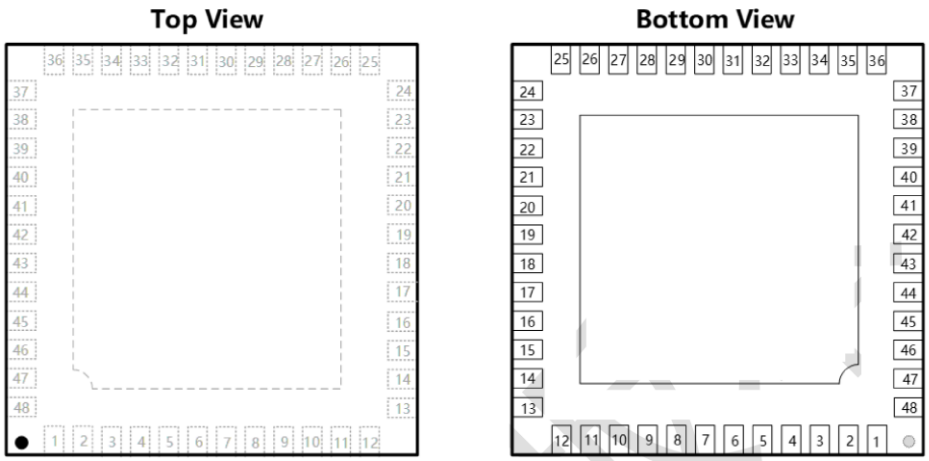
- Pole-pitch specification: main-track pole pitch is 2 mm; the vernier-track pole pitch is automatically matched by pole-pair count (1.3 mm / 1.66 mm / 1.83 mm).
- High resolution: built-in 22-bit angle-solver DSP, up to 4,194,304 absolute positions per single revolution.
- Multi-interface output: incremental ABZ quadrature pulses (up to 65,536 PPR), motor commutation UVW signals (1–64 pole pairs programmable), PWM, 4-wire SPI, and UART.
- Magnet ring compatibility: perfectly matched to 16-, 32- and 64-pole-pair dual-track magnet rings.
- Advanced self-calibration: built-in simple client self-calibration (compensates pole-pair magnetization offset) and constant-speed self-calibration (compensates eccentricity and mounting nonlinearity, achieving INL within ±0.1°).
- External magnetic field immunity: differential Hall sensing architecture provides strong active suppression of uniform external stray magnetic fields.
- Comprehensive diagnostics: supports magnetic-field out-of-range, motor overspeed, supply undervoltage, chip overtemperature and EEPROM CRC error alarms.
- Automotive reliability: meets AEC-Q100 Grade 1 (-40 °C to 125 °C), RoHS & REACH compliant, moisture sensitivity level MSL3.
- Programmable storage: built-in 3.3 V–5 V programmable EEPROM for power-off retention of user configuration.

1.3 Typical Applications

- Robot joints (hollow-shaft angle feedback in collaborative and humanoid robots)
- Absolute encoder systems for hollow-shaft motors and servo motors
- LiDAR rotary-stage angle monitoring
- High-precision linear displacement and magnetic scale measurement systems

2. Chip Pin Configuration

The NSM3502 is available in a QFN48 (7 mm × 7 mm, wettable flanks) package with 48 functional pins and one bottom thermal/ground exposed pad (EPAD 49). The table below lists the name, type and OTV Sensing evaluation-board connection of every pin.



NSM3502 封装

Pin	Symbol	Type	Function & Board Connection
1	HRST	Digital Input	Hardware reset. High >10 ms resets the chip; connected to button SW1 with a 10 kΩ pull-down
2	FAULT	Digital Output	Diagnostic alarm output, push-pull, active-high by default
3	PWM	Digital Output	PWM angle output, 12-bit resolution; connected to LED D1 on the board
4	CAL_EN	Digital Input	Client self-calibration enable; high triggers the self-calibration flow
5	AVDD	Power	Analog supply input (3.0–5.5 V); 100 nF decoupling capacitor on board
6	AGND	Power	Analog ground; single-point connected to DGND on board
7	A	Digital Output	Incremental quadrature A output (push-pull drive)
8	B	Digital Output	Incremental quadrature B output (push-pull drive)
9	Z	Digital Output	Incremental index Z output,

			programmable width (1–128 LSB)
10	U	Digital Output	UVW commutation U-phase output
11	V	Digital Output	UVW commutation V-phase output
12	W	Digital Output	UVW commutation W-phase output
13~25	NC	No Connect	Internally unconnected; tied to the PCB ground plane for shielding
26	TEST	Digital Input	Factory test pin; tied directly to ground on the board
27	MISO	Digital Output	SPI slave output; high-impedance (Hi-Z) when deselected
28	MOSI	Digital Input	SPI slave input; sampled on the SCLK rising edge
29	SCLK	Digital Input	SPI clock input; up to 16.6 MHz
30	CSN	Digital Input	SPI chip-select input, active low, with angle-latch function
31	DGND	Power	Digital ground; connected to the main ground plane
32	DVDD	Power	Digital supply input (3.0–5.5 V); 100 nF decoupling capacitor on board
33	VDDINT	Power Output	Internal LDO output (1.8 V); 1.8 nF internal, 1 µF external decoupling
34	RX	Digital Input	UART receive pin
35	REDE	Digital Output	UART transceiver direction-enable pin
36	TX	Digital Output	UART transmit pin
37~48	NC	No Connect	Internally unconnected; tied to the PCB ground plane for shielding
49	EPAD	Thermal Pad	Bottom exposed pad; connected to the ground plane for thermal and shielding

3. Specifications

This chapter collects all technical parameters from the NOVOSENSE NSM3502 datasheet, including electrical characteristics, EEPROM, digital I/O, ABZ/PWM signal specifications, input magnetic field, magnet-ring matching parameters and mechanical mounting tolerances.

3.1 Electrical Characteristics

Test conditions: ambient temperature TA = -40 °C to 125 °C, supply VDD = 3.3 V to 5.0 V, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating voltage range	VDD	3.0	3.3 ~ 5.0	5.5	V	Pins: AVDD, DVDD
Undervoltage alarm threshold	VTH_UV	-	2.55	-	V	Alarm when supply drops below this value
Undervoltage release threshold	VTH_POR	-	2.75	-	V	Power-on reset / undervoltage release
Operating current	Idd	-	50	-	mA	Typical full-function operating current
INL after factory calibration	INL(1)	-	±0.5	-	°	With 32-pole-pair ring, 0.6 mm air gap
INL after simple self-calibration	INL(2)	-	±0.3	-	°	With 32-pole-pair ring, after vernier trimming
INL after constant-speed self-calibration	INL(2)	-	±0.1	-	°	Typical accuracy after constant-speed calibration
Differential nonlinearity (full temp)	DNL	-	±0.005	-	°	Maximum DNL over full temperature
Transient noise	TN	-	0.01	-	°rms	25 °C, ABZ mode default bandwidth
Hysteresis window	HYST	0	0.022	0.7	°	Multi-level programmable via register
Power-up time	TPwrUP	-	50	-	ms	Power-up to stable output

System delay	TDelay	-	5	-	µs	Tracking delay in constant-speed rotation
Step response time	TST	-	300	-	µs	Default bandwidth configuration
Max speed (16 pole pairs)	Slimit	-	-	24,000	RPM	Guaranteed maximum speed
Max speed (32 pole pairs)	Slimit	-	-	12,000	RPM	Guaranteed maximum speed
Max speed (64 pole pairs)	Slimit	-	-	6,000	RPM	Guaranteed maximum speed

3.2 EEPROM & General Digital I/O

The NSM3502 has a built-in programmable EEPROM that persists user configuration across power cycles.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
EEPROM write endurance	N_ENDUR	10,000	-	-	cycles	Guaranteed erase/write cycles
EEPROM data retention	T_RET	20	-	-	years	At 85 °C
Digital I/O output low level	VOL	-	-	0.4	V	Push-pull (@Iout = -2 mA)
Digital I/O output high level	VOH	VDD-0.4	-	-	V	Push-pull (@Iout = 2 mA)
Signal rise time	TRise	-	-	50	ns	CL = 20 pF
Signal fall time	TFall	-	-	50	ns	CL = 20 pF

3.3 ABZ & PWM Output Parameters

ABZ encoding: 1 to 65,536 pulses per revolution (PPR) programmable; AB output maximum frequency 4.096 MHz. Note: when the frequency exceeds 4 MHz, the output integral nonlinearity (INL) may degrade.

PWM output: frequency programmable to 0.5 kHz, 1.0 kHz or 2.0 kHz (±5%); typical rise/fall time 1 µs (at CL = 1 nF); 12-bit PWM resolution (4096 steps).

3.4 Input Magnetic Field & Magnet Ring Specifications

The NSM3502 is matched to magnet rings with a fixed main-track pole pitch of 2.0 mm. The effective magnetic field strength Bpk perpendicular to the chip surface must be within 10 mT to 125 mT. For bonded ferrite magnet rings, the remanence temperature coefficient TKB is typically -0.19%/°C.

Parameter	Symbol	16 pole pairs	32 pole pairs	64 pole pairs	Unit
Chip-center to axis distance	DC_A	8.19	18.37	38.74	mm
Main-track diameter	Dmaster	20.37	40.74	81.49	mm
Vernier-track diameter	Dnonius	12.37	32.74	73.49	mm
Vernier-track pole pitch	Pnonius	1.30	1.66	1.83	mm

3.5 Mechanical Mounting Tolerance

Good mechanical mounting tolerance is the key to achieving the highest accuracy (INL < ±0.1°):

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Chip-to-ring surface distance (air gap)	AG	0.2	0.6	1.0	mm	Vertical working air-gap range
Radial alignment tolerance	DISPrad	-	-	0.5	mm	Radial mounting offset
Tangential alignment tolerance	DISPtan	-	-	0.5	mm	Tangential mounting offset
Ring eccentricity	DISP	-	-	0.1	mm	Magnet ring rotational eccentricity

4. Function Description & Communication Protocol

This chapter details the NSM3502 internal architecture, output modes (ABZ, UVW, PWM), SPI timing and protocol, CRC rules, EEPROM read/write flow, diagnostic alarm logic, direction control, and the 4-layer self-calibration algorithm.

4.1 Internal Architecture & Signal Processing

The NSM3502 integrates two high-sensitivity Hall sensor arrays (main track and vernier track). As the external magnet ring rotates, the arrays produce two pairs of sine and cosine analog voltages. These are amplified by a low-noise analog front-end (PGA) and low-pass filtered, then quantized by a high-resolution ADC. The DSP first calibrates offset, gain mismatch and phase error of the main/vernier tracks, then computes the respective electrical angles. Finally, the vernier synthesis algorithm

combines the two electrical angles into a 22-bit absolute mechanical angle over 360°. The absolute angle can be output directly via SPI, UART or PWM, or further synthesized into incremental ABZ and motor commutation UVW signals.

4.2 Incremental ABZ Output Mode

In ABZ mode, the chip outputs two quadrature pulses A and B with 90° phase difference, plus a zero-reference pulse Z. Resolution is programmed by the ABZ_RES[15:0] register (1 to 65,536 PPR, i.e. 262,144 edge steps per revolution). The Z signal represents the 0° mechanical position; its width can be programmed by Z_PUL_WID[3:0] to 1, 2, 4, 8, 16, 32, 64 or 128 LSB, or to 60°, 120° or 180° electrical angle. Z_EDGE and Z_PHASE align the Z pulse to the rising or falling edge of A/B. The chip establishes stable ABZ output about 50 ms after power-up.

4.3 UVW Commutation & PWM Output Mode

UVW commutation: the UVW mode outputs U, V and W signals mutually phase-shifted by 120°, used for electronic commutation of brushless DC (BLDC) motors. The pole-pair count is configured by UVW_RES[5:0] from 1 to 64 pole pairs.

PWM: the PWM output has a fixed period, with duty cycle proportional to the 12-bit absolute angle. Duty-cycle polarity is set by PWM_POL (active-high or active-low). PWM frequency is set by PWM_FREQ[1:0] (0.5 kHz / 1 kHz / 2 kHz).

4.4 SPI Interface Timing & Protocol

The NSM3502 provides a 4-wire SPI interface (CSN, SCLK, MOSI, MISO). Users can read the 22-bit absolute angle in real time, configure registers and program the EEPROM via SPI.

4.4.1 SPI Timing Specification

SPI communication is fixed to MODE 1 (CPOL = 0, CPHA = 1). SCLK idles low; the transmitter drives data on the rising edge and the receiver samples on the falling edge. Key timing parameters: TSCK (clock period) ≥ 60 ns (up to 16.6 MHz); TSCKL (low time) ≥ 30 ns; TSCKH (high time) ≥ 30 ns; TL (CSN falling edge to first SCLK rising edge) ≥ 100 ns; TH (last SCLK rising edge to CSN rising edge) ≥ 0.5 TSCK; TLATCH (CSN low-hold time required for angle latch) ≥ 1 µs.

4.4.2 SPI Operation Modes & Instruction Set

SPI data is transferred MSB-first. MISO is high-impedance (Hi-Z) when deselected. Each frame includes a 4-bit rolling counter (0x0–0xF) and 4-bit status flags S[3:0]. The chip has a read-only mode (Normal Mode, default after power-up) and a Service Mode.

Command	Opcode	MOSI Frame	MISO Frame	Bits	Description
NOP	000	Address/data ignored	24-bit 0 + 8-bit CRC	32-bit	No operation
General Read 1	001	8-bit address + 16-bit 0	16-bit data + 4-bit CNT + 4-bit Status + 8-bit CRC	32-bit	Generic single-address read
General Read 2	010	8-bit address (0xA0)	24-bit data (0xA0 &	32-bit	Continuous angle + high-

			upper 8 bits of 0xA1) + 8-bit CRC		bit read
Enter Service Mode	011	Key: 0x5E5A3E	Returns 0x5A3E0029 (Status=0, CRC=0x29)	32-bit	Enter service/write mode
Fast Read 1	100	0xA0 (ANG_RB)	24-bit Angle + 4-bit CNT + 4-bit Status + 8-bit CRC	40-bit	40-clock fast angle read
Fast Read 2	101	Start address	16-bit data + 4-bit CNT + 4-bit Status + 8-bit CRC	32-bit	Cyclic read of two consecutive addresses
General Write	100	8-bit address + 16-bit data	16-bit Echo + 4-bit CNT + 4-bit Status + 8-bit CRC	32-bit	Register write (Service Mode)
Exit Service Mode	111	Data ignored	16-bit Echo + 4-bit CNT + 4-bit Status + 8-bit CRC	32-bit	Exit service mode

4.4.3 22-Bit Absolute Angle Formula

The 22-bit absolute angle is stored at address 0xA0 (ANGLE_RB[21:6]) and 0xA1 (ANGLE_RB[5:0]). In the 24-bit angle data received via Fast Read 1, the upper 22 bits are the valid absolute angle binary value ANGLE_RB[21:0]; the lower 2 bits are padded with 0. The absolute angle θ (in degrees) is: $\theta = (\text{ANGLE\_RB}[21:0] / 2^{22}) \times 360°$.

4.4.4 CRC Mechanism

To guarantee reliable communication, both MOSI and MISO frames include CRC:

Host MOSI 5-bit CRC: polynomial x^5 + x^2 + 1 (0x12), initial seed 0x00, output not inverted; covers command, address and data (MSB first).

Slave MISO 8-bit CRC: polynomial x^8 + x^5 + x^3 + x^2 + x + 1 (0x97), initial seed 0xFF, output inverted (XOROUT = 0xFF).

4.4.5 EEPROM Operation Flow

Standard EEPROM programming: send the Enter Service Mode command → write 0x185E to address 0x86 to unlock write permission → modify target register → write 0x0000 to 0x86 to close write permission → write NVM_KEY (e.g. 0x5C) and the NVM_CTRL command (0x04: Byte-Program with erase, 0x03: Load, 0x0A: Erase) → read NVM_STA to confirm NVM_PROG_DONE.

4.5 Diagnostics & Alarms

The NSM3502 integrates a comprehensive diagnostic mechanism. The diagnostic result is recorded in the 16-bit DIAG_CODE[15:0] register. When any fault is detected and debounced, the FAULT pin outputs an active level (active-high by default; configurable via FAULT_POL). Debounce logic requires 16 consecutive fault cycles to set the alarm and 64 consecutive normal cycles to clear it (debounce time set by DIAG_DEBN_SET / CLR).

Fault Code	Enable Bit	Name	Description & Trigger Condition
DIAG_CODE[0]	DIAG_EN[0]	Main-track weak field	Main-track field below threshold RAD_TH_LO
DIAG_CODE[1]	DIAG_EN[1]	Main-track strong field	Main-track field above threshold RAD_TH_HI
DIAG_CODE[2]	DIAG_EN[2]	Vernier weak field	Vernier-track field below threshold RAD_TH_LO
DIAG_CODE[3]	DIAG_EN[3]	Vernier strong field	Vernier-track field above threshold RAD_TH_HI
DIAG_CODE[4]	DIAG_EN[4]	Overspeed alarm	Internal speed exceeds threshold MAX_VEL
DIAG_CODE[5]	DIAG_EN[5]	EEPROM CRC error	EEPROM load CRC verification failure
DIAG_CODE[8]	DIAG_EN[8]	Supply undervoltage	Supply below undervoltage threshold VTH_UV (2.55 V)
DIAG_CODE[9]	DIAG_EN[9]	Chip overtemperature	Internal temperature sensor above safe threshold

4.6 Rotation Direction Configuration

By default, looking from the top of the chip, counter-clockwise (CCW) magnet-ring rotation is the angle-increasing direction, with the B pulse leading the A pulse by 90° electrical. To reverse the direction, set ROT_DIR[0] to 1 (CW = increasing). This setting applies uniformly to ABZ, UVW, PWM, SPI and UART interfaces.

4.7 4-Layer Self-Calibration Algorithm

The NSM3502 uses a 4-layer calibration architecture to eliminate nonlinearity from the chip, magnet-ring magnetization offset and mechanical mounting:

- Layer 1 (factory calibration): performed by NOVOSENSE at factory test; calibrates Hall array offset, amplitude mismatch and temperature drift.
- Layer 2 (simple self-calibration): performed by the customer after assembly. Set the chip to simple mode (AUTO_CAL_MODE), rotate the ring over 16 pole pairs (40–3000 pole pairs/min,

constant speed not required). Pull CAL_EN high or write 0xB5 to AUTO_CAL_KEY; the chip auto-compensates magnetization non-uniformity, typically improving INL to within ±0.3°.

- Layer 3 (vernier trimming): fine-tune vernier-track error introduced by magnetization and mechanical mounting using a dedicated programming tool.
- Layer 4 (constant-speed self-calibration): after Layer 3 passes, rotate the ring at a stable constant speed (speed ripple must be < ±3‰). Pull CAL_EN high and rotate 64+ revolutions; the chip computes eccentricity and mounting nonlinearity and programs them into EEPROM. After success, INL drops to within ±0.1°. Read register 0xA3[1:0] for calibration status (00: idle, 01: running, 10: failed, 11: success).

4.8 Hardware Reset & Register Map

Reset: apply a high level to HRST (Pin 1) for more than 10 ms to trigger a hardware reset; hold low for more than 40 ms to release. If unused, the evaluation board ties HRST to ground through a 10 kΩ resistor.

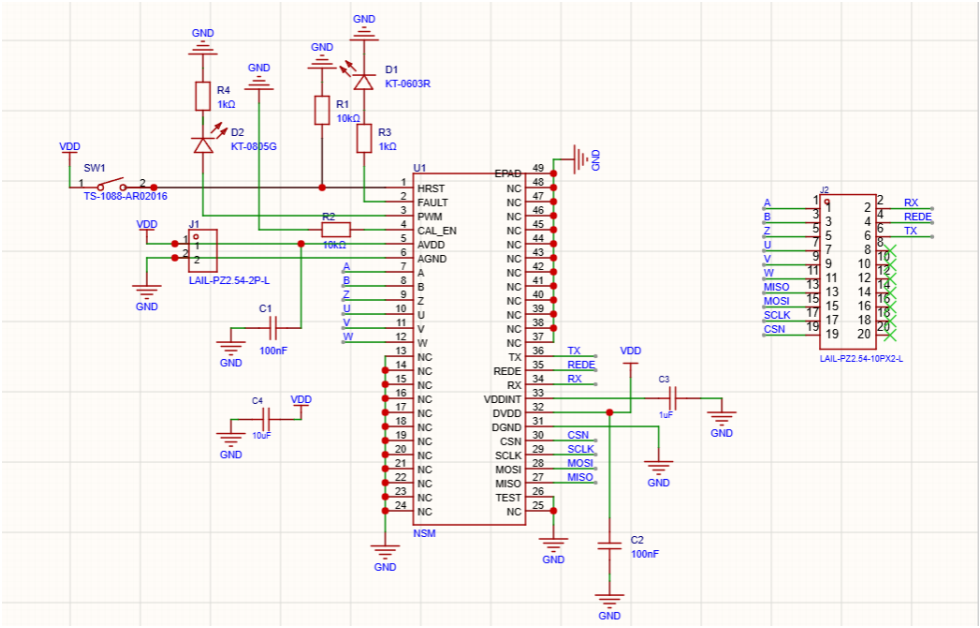
Address	Name	R/W	Default	Description
0x01E	USER_ID	RW	16'b0	User information record register
0x01F	ABZ_RES	RW	16'b0	ABZ resolution (0=1 ppr ~ 65535=65536 ppr)
0x020	UVW_RES	RW	6'b0	UVW resolution (0=1 ppr ~ 63=64 ppr)
0x020	ROT_DIR	RW	1'b0	Rotation direction (0: CCW, 1: CW)
0x020	Z_PUL_WID	RW	4'b0	Z pulse width (0=1 LSB ~ 7=180 deg)
0x021	PWM_FREQ	RW	2'b0	PWM frequency (0=1 kHz, 1=2 kHz, 2=0.5 kHz)
0x027	AUTO_CAL_MODE	RW	2'b0	Self-calibration mode (0/3: simple, 1: constant-speed, 2: simple+constant)
0x027	POLEPAIR_SEL	RW	2'b0	Pole-pair configuration (0/3: 32/31, 1: 16/15, 2: 64/63)
0x027	HYST	RW	4'b0	Angle hysteresis (15 levels)
0x02D	DIAG_EN	RW	16'b0	16-bit diagnostic alarm enable

				switches
0x02E	MAX_VEL	RW	2'b0	Speed alarm threshold (0:400 Hz, 1:200 Hz, 2:100 Hz, 3:600 Hz)
0x081	NVM_KEY	RW	8'b0	EEPROM programming key (0x5C / 0xB3)
0x081	NVM_CTRL	RW	5'b0	EEPROM command (0x04: Program, 0x03: Load)
0x082	AUTO_CAL_KEY	RW	8'b0	Write 0xB5 to trigger hardware auto-calibration
0xA0/0xA1	ANGLE_RB	RO	22-bit	Real-time read-only absolute mechanical angle (0xA0 high 16 bits, 0xA1 low 6 bits)
0xA2	NVM_STA	RO	8'b0	EEPROM status ([1]: Program Done, [2]: Fail)
0xA3	CAL_STATE	RO	2'b0	Calibration status (00: idle, 01: running, 10: failed, 11: success)
0xC8	DIAG_CODE	RO	16'b0	16-bit real-time diagnostic flag register

5. Evaluation Board Hardware Architecture

The OTV Sensing NSM3502 evaluation board strictly follows high-precision analog/digital mixed-signal design rules. The board contains the main chip U1 (NSM3502), supply decoupling circuitry, SW1 hardware reset button, LED status indicators (D1 calibration indicator, D2 power indicator), J1 2-pin power input terminal, and J2 20-pin standard dual-row header.

5.1 Board Schematic



5.2 Board Interface Pinout

The board is powered through J1 (2-pin, 2.54 mm terminal) and brings out all angle and communication signals through J2 (2×10, 20-pin, 2.54 mm dual-row header). The J2 header pinout is defined below:

Pin	Symbol	Type	Description	Pin	Symbol	Type	Description
1	A	Digital Output	Quadrature incremental A pulse	2	RX	Digital Input	UART receive
3	B	Digital Output	Quadrature incremental B pulse	4	REDE	Digital Output	UART direction enable
5	Z	Digital Output	Quadrature index Z pulse	6	TX	Digital Output	UART transmit
7	U	Digital Output	Motor commutation U phase	8	NC	No Connect	Reserved
9	V	Digital Output	Motor commutation V phase	10	NC	No Connect	Reserved
11	W	Digital Output	Motor commutation W phase	12	NC	No Connect	Reserved
13	MISO	Digital Output	SPI slave data output	14	GND	Power	System digital ground
15	MOSI	Digital Input	SPI slave data input	16	GND	Power	System digital

							ground
17	SCLK	Digital Input	SPI clock input	18	GND	Power	System digital ground
19	CSN	Digital Input	SPI chip select (active low)	20	GND	Power	System digital ground

6. Version History & Contact

Version	Release Date	Description
V1.0	2026.09	Initial release

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For any questions regarding evaluation board hardware, magnet ring selection or algorithm support, please contact the OTV Sensing technical team via the email above.